REMARKS/ARGUMENTS

Initially, Applicants would like to express appreciation to the Examiner for the detailed Official Action provided, for the acknowledgment of Applicants' Information Disclosure Statement by return of the Form PTO-1449, and for the acknowledgment of Applicants' Claim for Priority and receipt of the certified copy of the priority document in the Official Action. However, Applicants note that the Examiner has not acknowledged that the drawings are acceptable, and it is requested that the Examiner indicate the same in the next Official Action.

Upon entry of the above amendments, claim 1 will have been amended and claim 2 will have been canceled without prejudice or disclaimer to the subject matter contained therein, and claims 3 and 4 will have been added. Claims 1, 3 and 4 are currently pending. Applicants respectfully request reconsideration of the outstanding rejection, and allowance of all the claims pending in the present application.

Initially, Applicants note that in the Official Action, the Examiner has rejected claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over NIHONMATSU et al. (U.S. Publication No. 2003/0171075) in view of HASHII et al. (U.S. Publication No. 2002/0016072).

Without acquiescing to the propriety of the Examiner's rejections, Applicants have amended independent claim 1 solely in order to expedite prosecution of the present application.

In this regard, Applicants note that NIHONMATSU and HASHII, alone or in any properly reasoned combination, lack any disclosure of the elements recited in claim 1.

In particular, claim 1 sets forth a method for manufacturing a wafer including, inter alia, the top surface polishing of the semiconductor wafer being performed at a different speed than the back surface polishing of the semiconductor wafer, and...wherein the etching of the semiconductor wafer comprises a first acid etching using a first acid etching solution on the semiconductor wafer, then a second acid etching using a second acid etching solution on the semiconductor wafer, and then alkali etching the semiconductor wafer.

Applicants submit that NIHONMATSU and HASHII, alone or in any properly reasoned combination, lack any disclosure of at least the aforementioned combination of elements.

In setting forth the rejection, the Examiner asserts that NIHONMATSU discloses the general method of manufacturing a surface of a wafer including a composite etching comprising both acid and alkali etching.

However, the Examiner acknowledges that NIHONMATSU does not disclose simultaneously polishing top and back surfaces of the wafer.

Nevertheless, the Examiner takes the position that it would be obvious to supply the acknowledged deficiencies of NIHONMATSU with the purported teachings of HASHII.

Initially, Applicants note that HASHII discloses polishing both surfaces simultaneously. However, in the method disclosed in HASHII, both surfaces of the semiconductor wafer receive a mirror polish. In other words, HASHII does not contemplate the polishing speed on the top surface of the wafer being different from the

polishing spead on the back surface of the wafer, as discussed on page 11, lines 11-18, of the present Specification.

In this regard, Applicants submit that at least one advantage of the presently claimed invention is that, because the polishing speed on the top surface of the wafer is different from the polishing speed on the back surface of the wafer, it is possible to obtain (in one operation) polished top and back surfaces each having a different gloss value; thereby allowing the top and back surfaces of the wafer to be distinguishable from each other (e.g., through visual inspection).

Further, Applicants submit that NIHONMATSU discloses performing alkali etching before performing acid etching (see, paragraph [0062] of NIHONMATSU). That is, NIHONMATSU does not disclose performing acid etching before alkali etching; much less, performing a first acid etching on the semiconductor wafer, a second acid etching on the semiconductor wafer, and then an alkali etching on the semiconductor wafer, as generally recited in claim 1.

Thus, NIHONMATSU and HASHI, alone or in any properly reasoned combination, fail to disclose at least the presently claimed top surface polishing of the semiconductor wafer being performed at a different speed than the back surface polishing of the semiconductor wafer; or performing a first acid etching on the semiconductor wafer, a second acid etching on the semiconductor wafer, and then an alkali etching on the semiconductor wafer, as generally recited in claim 1.

Further, Applicants submit that newly added independent claim 3, is generally somewhat similar to independent claim 1 in that it recites a method for manufacturing a semiconductor wafer including, inter alia, top surface polishing of the semiconductor

wafer being performed at a different speed than the back surface polishing of the semiconductor wafer, and...wherein the etching of the semiconductor wafer comprises an alkali etching on the semiconductor wafer, then an acid etching on the semiconductor wafer; and wherein an amount of the alkali etching relative to an amount of the acid etching is in a ratio of 3:2.

Further, Applicants submit that newly-added independent claim 4, is generally somewhat similar to independent claim 1 in that it recites a method for manufacturing a semiconductor wafer including, inter alia, top surface polishing of the semiconductor wafer being performed at a different speed than the back surface polishing of the semiconductor wafer, and...the etching of the semiconductor wafer comprises a first acid etching using a first acid etching solution on the semiconductor wafer, then alkali etching the semiconductor wafer, and then a second acid etching using a second acid etching solution on the semiconductor wafer.

Accordingly, amended independent claim 1, as well as newly-added independent claims 3 and 4, are each patentable over the applied prior art.

In view of the amendments and arguments herein, Applicants submit that independent claims 1, 3 and 4 are each in condition for allowance.

Thus, it is respectfully submitted that all of the claims in the present application are clearly patentable over the references cited by the Examiner, either alone or in combination, and an indication to such effect is respectfully requested, in due course.

SUMMARY

Applicants submit that the present application is in condition for allowance, and respectfully request an indication to that effect. Applicants have argued the allowability of the claims and pointed out deficiencies of the applied references. Accordingly, reconsideration of the outstanding Official Action and allowance of the present application and all the claims therein are respectfully requested and is now believed to be appropriate.

Applicants note that this amendment is being made to advance prosecution of the application to allowance, and should not be considered as surrendering equivalents of the territory between the claims prior to the present amendment and the amended claims. Further, no acquiescence as to the propriety of the Examiner's rejection is made by the present amendment. All other amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability.

Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,

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